CLAIMS

WHAT IS CLAIMED IS:

1. A probe head comprising:

a substrate having a first surface and an opposing second surface;

a conductive plane embedded within said substrate;

a plurality of terminals disposed on said first surface

a plurality of signal pads disposed on said second surface and electrically connected to said plurality of terminals; and

a conductive area disposed on said second surface between ones of said signal pads and electrically connected to said conductive plane, said conductive area being electrically insulated from said plurality of signal pads.

2. The probe head of claim 1 wherein said conductive area comprises a conductive plane.

3. The probe head of claim 2, wherein said conductive plane comprises a plurality of openings in which are disposed said plurality of signal pads.

4. The probe head of claim 3, wherein each said opening provides a space between said signal pad disposed therein and said conductive plane in a range of 2 to 20 mils.

5. The probe head of claim 2, wherein said plurality of signal pads are disposed in a two-dimensional array.

6. The probe head of claim 5, wherein said plurality of signal pads are disposed at a pitch in a range of 20 to 100 mils.

7. The probe head of claim 1, wherein said conductive area comprises a plurality of ground pads.

8. The probe head of claim 7, wherein at least one signal pad is disposed between each of said plurality of ground pads.

9. The probe head of claim 7, wherein said plurality of signal pads are disposed in a two-dimensional array.

10. The probe head of claim 9, wherein adjacent signal pads are spaced from each other in a range of 2 to 15 mils.

11. The probe head of claim 9, wherein said plurality of signal pads are disposed at a pitch in a range of 15 to 50 mils.

12. The probe head of claim 7, wherein said plurality of signal pads and said plurality of ground pads are disposed on said second surface of said substrate in a pattern comprising:

a subpattern comprising a ground pad disposed between at least two signal pads; and

a two-dimensional array of said subpattern.

13. The probe head of claim 12, wherein said subpattern comprises a ground pad disposed between four signal pads.

14. A method of making a probe card assembly comprising:

providing a first component of said probe card assembly as a premanufactured component, said first component comprising a substrate and a first patterned conductive layer on a first surface of said substrate, said first patterned conductive layer comprising:

a plurality of signal pads electrically connected to a plurality of terminals disposed on a second surface of said substrate, and

a conductive area electrically connected to a conductive plane embedded within said substrate, said plurality of signal pads being electrically insulated from said conductive area and said embedded plane;

thereafter receiving design data regarding a semiconductor device to be tested by said probe card assembly, said design data including locations of test points on said semiconductor device,

forming a plurality of contact element pads on said first electronic component disposed to correspond to said locations of said test points on said semiconductor device and electrically connected to a first subset of said signal pads;

electrically connecting a signal pad from a second set of said signal pads to said conductive area; and

adding a plurality of contact elements for contacting said test points on said semiconductor device to said plurality of contact element pads.

15. The method of claim 14, wherein said conductive area comprises a ground plane.

16. The method of claim 15, wherein said ground plane comprises a plurality of openings in which are disposed said plurality of signal pads.

17. The method of claim 14, wherein said conductive area comprises a plurality of ground pads.

18. The method of claim 14 further comprising:

forming a plurality of electronic component pads on said first electronic component; and

disposing at least one electronic component on said plurality of pads.

19. The method of claim 18, wherein said at least one electronic component is a capacitor.

20. The method of claim 14 further comprising electrically connecting a plurality of signal pads from said second set of said signal pads to said conductive area.

21. The method of claim 14, wherein at least one of said test points protrudes from a surface of said semiconductor device, and said plurality of contact elements includes at least one corresponding contact element configured to contact said protruding test point.

22. The method of claim 21, wherein said at least one corresponding contact element is selected from a group consisting of a pad, a recess, and a socket.

23. The method of claim 14 further comprising combining said first component with at least one other component to form said probe card assembly.

24. The method of claim 23, wherein said at least one other component is one of a printed circuit board configured to make electrical connections with a semiconductor tester, an interposer, and an interface with a cable from a semiconductor tester.

25. The method of claim 14 further comprising forming an insulating layer over said first patterned conductive layer, and forming said plurality of contact element pads on said insulating layer.

26. A probe head comprising:

a substrate having a first surface and an opposing second surface;

a plurality of terminals disposed on said second surface; and

a plurality of signal pads electrically connected to said plurality of terminals and disposed on said first surface in a pattern in which a spacing between adjacent ones of at least some of said signal pads varies with a location of one of said adjacent pads on said first component.

27. The probe head of claim 26, wherein said spacing between adjacent ones of said at least some of said plurality of pads increases with a distance of said pad from a reference location on said substrate.

28. The probe head of claim 26, wherein a size of said at least some of said plurality of pads varies with a location of said pads on said substrate.

29. The probe head of claim 28, wherein said size of said at least some of said plurality of signal pads increases with a distance of said pads from a reference location on said substrate.

30. A method of making a probe card assembly comprising:

providing a first component of said probe card assembly as a premanufactured component, said first component comprising a plurality of signal pads at least some of whose spacing from an adjacent pad varies with a location of said signal pad on said first component;

thereafter receiving design data regarding a semiconductor device to be tested by said probe card assembly, said design data including locations of test points on said semiconductor device,

forming a plurality of contact element pads on said first electronic component disposed to correspond to said locations of said test points on said semiconductor device, ones of said contact element pads being electrically connected to ones of said plurality of signal pads; and

adding a plurality of contact elements for contacting said test points on said semiconductor device to said plurality of contact element pads.

31. The method of claim 30 further comprising combining said first component with at least one other component to form said probe card assembly.

32. The method of claim 31, wherein said at least one other component is one of a printed circuit board configured to make electrical connections with a semiconductor tester, an interposer, and an interface with a cable from a semiconductor tester.

33. The method of claim 30, wherein at least one of said test points protrudes from a surface of said semiconductor device, and said plurality of contact elements includes at least one corresponding contact element configured to contact said protruding test point.

34. The method of claim 31, wherein said at least one corresponding contact element is selected from a group consisting of a pad, a recess, and a socket.

35. The method of claim 30, wherein a size of said at least some of said plurality of pads varies with a location of said pad on said first component.

36. The method of claim 35, wherein said size of said at least some of said plurality of signal pads increases with a distance of said pad from a reference location on said first component.

37. The method of claim 30, wherein said spacing between adjacent ones of said at least some of said plurality of pads increases with a distance of said pad from a reference location on said first component.